Notice of Allowability	Application No.	Applicant(s)	
	10/759,193	YAMADA ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 1/19/07*.

2. ☒ The allowed claim(s) is/are *1,5-8,10,11 and 21-25*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Paul Skwierawski (Reg. No. 32,173) on 10 May 2007.

The application has been amended as follows:

- Please amend claim 1 to read:

"A modular computer system formed by connecting a processing module having a processor mounted thereon and a plurality of I/O modules in a stacked form via connectors, where differing ones of the plurality of I/O modules being differing types of I/O modules from one another, which operate with mutually differing types of bus-layout configurations, and where at least a portion of said connectors representing a reconfigurable generic bus, wherein

each I/O module comprises:

an I/O module connector representing one of the connectors;

a module exclusive selection part for activating the module responsive to a module select signal input from a terminal in a predetermined position on a processing module side connector, the predetermined position being the same for said I/O modules; and

an ID output part for outputting identification information of its own I/O module to at least one predetermined terminal on the I/O module connector on the basis of the module select signal output from said module exclusive selection part;

wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected; and

an ID input part for taking in the identification information output to the at least one predetermined terminal on the I/O module connector,

where said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing module, and

said ID input part recognizes the I/O modules and the identification information in association with an output order of the module select signal; and

wherein in accordance with the association of the I/O modules with the identification information, for each differing type of I/O module stacked via the connectors, said processing module selects from differing preset bus-layout configurations and device drivers from a memory, to dynamically reconfigure the reconfigurable generic bus for accessing the differing type of I/O module."

- Please amend claim 11 to read:

"The modular computer system according to claim 21, wherein said ID output part is formed by connecting wires driven by the activate signal to a plurality of predetermined terminals on the input connector via PN-junction elements according to the identification information."

- Please amend claim 22 to read:

"A modular computer system formed by connecting a processing module having a processor mounted thereon and a plurality of I/O modules in a stacked form via connectors, where differing ones of the plurality of I/O modules being differing types of I/O modules from one another, which operate with mutually differing types of bus-layout configurations, and where at least a portion of said connectors representing a reconfigurable generic bus, wherein

each I/O module comprises:

a module exclusive selection part for activating the module responsive to a module select signal input from a terminal in a predetermined position on a processing module side connector; and

an ID output part for outputting identification information of its own I/O module to at least one predetermined terminal on the processor module side connector on the basis of the module select signal output from said module exclusive selection part;

wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected; and

an ID input part for taking in the identification information output to the at least one predetermined terminal on the processor module side connector,

where said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing module, and

said ID input part recognizes the I/O modules and the identification information in association with an output order of the module select signal; and

wherein in accordance with the association of the I/O modules with the identification information, for each differing type of I/O module stacked via the connectors, said processing module selects from differing preset bus-layout configurations and device drivers from a memory, to dynamically reconfigure the reconfigurable generic bus for accessing the differing type of I/O module."

- Please amend claim 23 to read:

" The modular computer system according to claim 1, wherein said processing module selects from differing preset bus timing sequences from the memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus."

- Please amend claim 24 to read:

" The modular computer system according to claim 21, wherein said processing module selects from differing preset bus timing sequences from the memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus."

- Please amend claim 25 to read:

" The modular computer system according to claim 22, wherein said processing module selects from differing preset bus timing sequences from the memory, to dynamically reconfigure a timing sequence operational on the reconfigurable generic bus."

DETAILED ACTION

2. Claims 1, 5 – 8, 10 – 11, and 22 – 25 are pending.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19 January 2007 has been entered.

Allowable Subject Matter

4. Claims 1, 5 – 8, 10 – 11, and 22 – 25 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Claims 1 and 23 are allowed because the prior art of record fails to teach or suggest alone or in combination ***dynamically reconfiguring a reconfigurable generic bus for accessing differing types of I/O modules***, as required by independent claim 1, ***in combination with the other recited claim limitations*** (emphasis added). "*Dynamically reconfigurable*" has been determined to mean reconfigurable while the system is operating under normal conditions. Applicant has argued the deficiencies of the prior art in the response filed 19 January 2007 at Page 12 Paragraph 3 – Page 13 Paragraph 2. Support for this limitation is found in the originally filed specification at Page 17 Line 14 – Page 18 Line 14 and Page 19 Line 25 – Page 20 Line 22. The prior art of record, US Patent No 4,727,475 (hereinafter Kiremidjian), teaches the use of a consistent bus (Kiremidjian; Figure 3 Item 11) but and does not teach that the bus is

dynamically reconfigurable. US Patent No. 6,003,097 (hereinafter Richman) teaches the use of bus configuration drivers (Richman; Col 6 Lines 51 – 64) but does not teach dynamically reconfiguring a reconfigurable bus.

Claims 5 – 8, 10 – 11, 21, and 24 are allowed because the prior art of record fails to teach or suggest alone or in combination ***dynamically reconfiguring a reconfigurable generic bus for accessing differing types of I/O modules***, as required by independent claim 21, ***in combination with the other recited claim limitations*** (emphasis added). "*Dynamically reconfigurable*" has been determined to mean reconfigurable while the system is operating under normal conditions. Applicant has argued the deficiencies of the prior art in the response filed 19 January 2007 at Page 12 Paragraph 3 – Page 13 Paragraph 2. Support for this limitation is found in the originally filed specification at Page 17 Line 14 – Page 18 Line 14 and Page 19 Line 25 – Page 20 Line 22. The prior art of record, US Patent No 4,727,475 (hereinafter Kiremidjian), teaches the use of a consistent bus (Kiremidjian; Figure 3 Item 11) but and does not teach that the bus is dynamically reconfigurable. US Patent No. 6,003,097 (hereinafter Richman) teaches the use of bus configuration drivers (Richman; Col 6 Lines 51 – 64) but does not teach dynamically reconfiguring a reconfigurable bus.

Claims 22 and 25 are allowed because the prior art of record fails to teach or suggest alone or in combination ***dynamically reconfiguring a reconfigurable generic bus for accessing differing types of I/O modules***, as required by independent claim

22, ***in combination with the other recited claim limitations*** (emphasis added). "*Dynamically reconfigurable*" has been determined to mean reconfigurable while the system is operating under normal conditions. Applicant has argued the deficiencies of the prior art in the response filed 19 January 2007 at Page 12 Paragraph 3 – Page 13 Paragraph 2. Support for this limitation is found in the originally filed specification at Page 17 Line 14 – Page 18 Line 14 and Page 19 Line 25 – Page 20 Line 22. The prior art of record, US Patent No 4,727,475 (hereinafter Kiremidjian), teaches the use of a consistent bus (Kiremidjian; Figure 3 Item 11) but and does not teach that the bus is dynamically reconfigurable. US Patent No. 6,003,097 (hereinafter Richman) teaches the use of bus configuration drivers (Richman; Col 6 Lines 51 – 64) but does not teach dynamically reconfiguring a reconfigurable bus.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
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Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER